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## PALM INTRANET

### Inventor Name Search Result

Your Search was:

Last Name = TRAN

First Name = DZUNG

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">08577875</a>	<a href="#">5796951</a>	150	12/22/1995	SYSTEM FOR DISPLAYING INFORMATION RELATING TO A COMPUTER NETWORK INCLUDING ASSOCIATING DEVICES WITH TASKS PERFORMABLE ON THOSE DEVICES	TRAN, DZUNG
<a href="#">09016810</a>	<a href="#">5960439</a>	150	01/30/1998	DEFINING A SCHEMA FOR A DATABASE REPRESENTING A MODEL OF A COMPUTER NETWORK	TRAN, DZUNG
<a href="#">09987168</a>	<a href="#">7213263</a>	150	11/13/2001	SYSTEM AND METHOD FOR SECURE NETWORK MOBILITY	TRAN, DZUNG
<a href="#">10170943</a>	Not Issued	161	06/12/2002	Content server	TRAN, DZUNG
<a href="#">10830033</a>	<a href="#">7337920</a>	150	04/23/2004	FLUID DISPENSING APPARATUS	TRAN, DZUNG
<a href="#">10948988</a>	Not Issued	120	09/24/2004	Emulated universal serial bus input devices	TRAN, DZUNG
<a href="#">11025116</a>	Not Issued	61	12/29/2004	Remote USB network device control	TRAN, DZUNG
<a href="#">11025130</a>	Not Issued	61	12/29/2004	Remote USB videophone communication	TRAN, DZUNG
<a href="#">60247008</a>	Not Issued	159	11/13/2000	System for computer network mobility	TRAN, DZUNG
<a href="#">10737141</a>	Not Issued	71	12/15/2003	System and method for intelligent transcoding	TRAN, DZUNG D.
<a href="#">09016865</a>	<a href="#">6076106</a>	150	01/30/1998	USER INTERFACE FOR DISPLAYING INFORMATION ABOUT A COMPUTER NETWORK	TRAN, DZUNG D.
<a href="#">60276389</a>	Not	159	03/16/2001	Flip-flop	TRAN, DZUNG J.

	Issued				
<a href="#">60299547</a>	Not Issued	159	06/19/2001	Flip-flop with uniform propagation delay	TRAN, DZUNG J.
<a href="#">60622929</a>	Not Issued	159	10/27/2004	Unconventional clocked circuit components having multiple timing models	TRAN, DZUNG J.
<a href="#">07509904</a>	<a href="#">5040139</a>	150	04/16/1990	TRANSMISSION GATE MULTIPLEXER (TGM) LOGIC CIRCUITS AND MULTIPLIER ARCHITECTURES	TRAN, DZUNG J.
<a href="#">07510114</a>	<a href="#">5200907</a>	250	04/16/1990	TRANSMISSION GATE LOGIC DESIGN METHOD	TRAN, DZUNG J.
<a href="#">07553891</a>	Not Issued	161	07/16/1990	TRANSMISSION GATE MULTIPLEXER (TGM) LOGIC CIRCUITS AND MULTIPLIER ARCHITECTURES	TRAN, DZUNG J.
<a href="#">07670075</a>	<a href="#">5162666</a>	195	03/15/1991	TRANSMISSION GATE SERIES MULTIPLEXER	TRAN, DZUNG J.
<a href="#">08538743</a>	Not Issued	161	10/02/1995	METHOD OF MINIMIZING LOGIC USING SERIAL MULTIPLEXERS	TRAN, DZUNG J.
<a href="#">08572052</a>	Not Issued	161	12/14/1995	HIGH-SPEED DYNAMIC LOGIC	TRAN, DZUNG J.
<a href="#">08595556</a>	Not Issued	161	02/01/1996	TAPPED SERIAL MULTIPLEXERS	TRAN, DZUNG J.
<a href="#">08695068</a>	<a href="#">5796128</a>	250	07/25/1996	GATE ARRAY WITH FULLY WIRED MULTIPLEXER CIRCUITS	TRAN, DZUNG J.
<a href="#">08708132</a>	Not Issued	161	08/26/1996	PARALLEL DYNAMIC LOGIC CIRCUIT	TRAN, DZUNG J.
<a href="#">09537969</a>	<a href="#">6356112</a>	250	03/28/2000	Exclusive or/nor circuit	TRAN, DZUNG JOSEPH
<a href="#">09888000</a>	Not Issued	168	06/21/2001	Flip-flop with slave-first clocking scheme	TRAN, DZUNG JOSEPH
<a href="#">09939348</a>	<a href="#">6480054</a>	250	08/24/2001	DIGITAL ELECTRONIC CIRCUIT FOR USE IN IMPLEMENTING DIGITAL LOGIC FUNCTIONS	TRAN, DZUNG JOSEPH
<a href="#">10010259</a>	<a href="#">6469541</a>	250	12/05/2001	EXCLUSIVE OR/NOR CIRCUIT	TRAN, DZUNG JOSEPH
<a href="#">10017303</a>	Not Issued	161	12/13/2001	Flip-flop with advantageous timing	TRAN, DZUNG JOSEPH
<a href="#">10145068</a>	Not Issued	161	05/13/2002	Unconventional clocked circuit components having multiple	TRAN, DZUNG JOSEPH

				timing models	
<a href="#">10293189</a>	Not Issued	161	11/12/2002	Digital electronic circuit for use in implementing digital logic functions	TRAN, DZUNG JOSEPH
<a href="#">08779012</a>	<a href="#">5859547</a>	150	12/20/1996	DYNAMIC LOGIC CIRCUIT	TRAN, DZUNG JOSEPH
<a href="#">08808249</a>	<a href="#">5780883</a>	250	02/28/1997	GATE ARRAY ARCHITECTURE FOR MULTIPLEXER BASED CIRCUITS	TRAN, DZUNG JOSEPH
<a href="#">09228149</a>	Not Issued	161	01/11/1999	DYNAMIC LOGIC CIRCUIT	TRAN, DZUNG JOSEPH
<a href="#">09348994</a>	<a href="#">6184718</a>	250	07/07/1999	DYNAMIC LOGIC CIRCUIT	TRAN, DZUNG JOSEPH
<a href="#">09477153</a>	<a href="#">6288593</a>	250	01/04/2000	DIGITAL ELECTRONIC CIRCUIT FOR USE IN IMPLEMENTING DIGITAL LOGIC FUNCTIONS	TRAN, DZUNG JOSEPH
<a href="#">09528857</a>	<a href="#">6313664</a>	150	03/20/2000	Load capacitance compensated buffer, apparatus and method thereof	TRAN, DZUNG T.
<a href="#">10747748</a>	<a href="#">7002371</a>	150	12/29/2003	LEVEL SHIFTER	TRAN, DZUNG T.
<a href="#">10926121</a>	<a href="#">7095246</a>	150	08/25/2004	VARIABLE IMPEDANCE OUTPUT BUFFER	TRAN, DZUNG T.
<a href="#">11360724</a>	Not Issued	120	02/23/2006	Electronic device and method	TRAN, DZUNG T.
<a href="#">11424132</a>	Not Issued	41	06/14/2006	LOW VOLTAGE CIRCUIT WITH VARIABLE SUBSTRATE BIAS	TRAN, DZUNG T.
<a href="#">11460349</a>	Not Issued	41	07/27/2006	VOLTAGE CONTROL CIRCUIT HAVING A POWER SWITCH	TRAN, DZUNG T.
<a href="#">11532295</a>	Not Issued	30	09/15/2006	PERFORMANCE VARIATION COMPENSATING CIRCUIT AND METHOD	TRAN, DZUNG T.
<a href="#">11561209</a>	Not Issued	71	11/17/2006	LATCHING INPUT BUFFER CIRCUIT WITH VARIABLE HYSTERESIS	TRAN, DZUNG T.
<a href="#">12004617</a>	Not Issued	17	12/21/2007	Input buffer	TRAN, DZUNG T.
<a href="#">09128164</a>	<a href="#">6263424</a>	250	08/03/1998	EXECUTION OF DATA DEPENDENT ARITHMETIC INSTRUCTIONS IN MULTI-PIPELINE PROCESSORS	TRAN, DZUNG X.

<a href="#">09274275</a>	<a href="#">6172623</a>	250	03/22/1999	EFFICIENT BIT SCAN MECHANISM	TRAN, DZUNG X.
<a href="#">09276427</a>	<a href="#">6304956</a>	250	03/25/1999	USING TWO BARREL SHIFTERS TO IMPLEMENT SHIFT, ROTATE, ROTATE WITH CARRY, AND SHIFT DOUBLE AS SPECIFIED BY THE X86 ARCHITECTURE	TRAN, DZUNG X.
<a href="#">90006051</a>	Not Issued	195	07/03/2001	TRANSMISSION GATE SERIES MULTIPLEXER	TRANSLOGIC TECH., INC. (OWNER). DZUNG JOSEPH TRAN.

**Inventor Search Completed:** No Records to Display.

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